REMARKS

The Applicant has filed the present Response in reply to the outstanding Official Action of September 21, 2004, and the Applicant believes the Response to be fully responsive to the Official Action for reasons set forth below in greater detail.

At the onset, the Applicant would like to note that Claims 5 and 6 have been amended to overcome the Examiner's rejection of the claims under 35 U.S.C. § 112, second paragraph. The phrase "where i is a natural number not more than n" is specifically recited.

In the outstanding Official Action, the Examiner rejected Claims 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Kawai et al. (U.S. Patent No. 4,953,128) (hereinafter "Kawai"). With regard to Claim 5, the Examiner asserts that Kawai discloses a coincidence detecting circuit comprising XOR gates and a NOR gate. Each of the XOR gates has two inputs. The NOR outputs an RS signal. The Examiner contends that although the reference does not teach an OR gate, it would have been obvious to one of ordinary skill in the art to replace the NOR gate with an OR gate. The Examiner asserts that one would have been motivated to implement such a replacement because using a NOR gate verses an OR gate would depend on the necessity of an inversion on the output of such a gate. The Examiner rejects Claim 6 using the same argument substituting a AND gate for the XOR gate.

The Applicant respectfully disagrees with the Examiner rejection and traverses the rejection with at least the following reasons.

The reference fails to teach that the I-th comparator inverts the I-th digital result signal at a timing indicated by said clock signal while the 2i-1-th input signal and the 2i-th input signal coincide with each other and does not invert said digital result signal while the 2i-1-th input signal and the 2i-th input signal do not coincide with each other, as recited in the claims.

In the claimed invention, the inversion of the result signal RESULT indicates that the data analyzer 30a has no failure. According to the first embodiment of the invention, if the result signal RESULT is inverted for every rise of the clock signal CLK, it proves that the output pattern DOUT and the expected pattern DATAE perfectly coincide with each other so that both the semiconductor circuit targeted for the test and the comparator 10 are normally operated.

On the other hand, if the result signal RESULT is inverted for each rise of the clock signal CLK in a certain period and not inverted even after the rise of the clock signal CLK in another period, it indicates that the tested semiconductor circuit has a failure while although the comparator 10 is normal. If the comparator 10 has a failure, it cannot be considered that the operation for inverting the result signal RESULT for each rise of the clock signal CLK is carried out even in the transient manner.

Also, if the result signal RESULT is not inverted at all even after the rise of the clock signal CLK, it is not possible to judge which of the tested semiconductor circuit and the comparator 10 has any failures. In order to determine which of the tested semiconductor circuit and the comparator 10 has any failures, it is necessary to judge by inspecting each of them. In this embodiment, it is only this case that requires the separate inspection with regard to the tested semiconductor circuit and the comparator 10, in order to determine which of the tested semiconductor circuit and the comparator 10 has any failures.

According to the second embodiment, the operation of the data analyzer enables to prove not only that the input signals X_1 to X_N are at the predetermined state but also that the data analyzer 30 has no failure. If the result signal RESULT is **inverted** for each rise of the clock signal CLK, it indicates that the input signals X_1 to X_N are at the predetermined state and the data analyzer 30 has no failure. If there is the period in which the total result signal RESULT ALL is not inverted even after the rise of the clock signal CLK, it proves that one of the DRAM 22a and the SRAM 22b has a failure.

Therefore, in each embodiment, inversion of the result signal at a clock signal is used to determine if there is a failure or not. Not only does the prior art fail to teach inversion of the result signal at a timing indicated by a clock, but also its use in determining a failure.

The circuit disclosed in Kawai will not solve the need to provide a comparing circuit in which it is possible to eliminate the possibility that comparison signals are recognized to be identical because of a failure of the comparing circuit. The coincidence circuit of Kawai would still result in a false positive.

Accordingly, Kawai fails to teach, suggest or render obvious all of the limitations of Claims 5 and 6.

The Applicant would also like to note that Claims 15-18 have been added to the application for examination. Applicant respectfully submits that Claims 15-18 are patentably distinct from the cited reference for at least the same reasons as identified above. Claims 15 and 16 are dependant either directly or indirectly from Claim 5 and Claims 17 and 18 are dependant either directly or indirectly from Claim 6. These claims are directed to structural components of the I-th comparator. Specifically, the I-th comparator includes at least a logic circuit and a flip-flop. The logic circuit outputs a control signal to the flip-flop so as to indicate inversion or non-inversion of the storage datum. Support for the additional claims can be found at pages 14-15 of the disclosure, i.e. "The comparator 10 includes the logic circuit 1 and a flip-flop 2." See also Figure 2, Figure 8 and Figure 9.

Kawai fails to teach both the claimed circuit structure and function. Specifically, the reference fails to teach at least that the logic circuit outputs the flip-flop input signal so as to indicate an inverse of the storage datum while said (2i-1)-th input signal and the

2i-th input signal coincide with each other, and outputs the flip-flop input signal so as to indicate the storage datum while said (2i-1)-th input signal and the 2i-th input signal do not coincide with each other as specifically claimed in claims 15 and 17.

Additionally, with regard to Claims 16 and 18, the reference fails to teach an exclusive OR gate outputting the flip-flop input signal so as to indicate an exclusive OR of the inverted signal and the (2i-1)-th input signal and the 2i-th input signal as specifically claimed.

Lastly, Claims 1-4, and 7-14 have been withdrawn from present consideration by the prior response to the restriction filed on June 18, 2004. The claims have been designated as withdrawn above.

For all the foregoing reasons, the Applicant respectfully requests the Examiner to withdraw the rejections of independent Claims 5-6 pursuant to 35 U.S.C. § 103(a). Furthermore, the Applicant respectfully submits that new Claims 15-18 are patentably distinct from the cited reference.

In conclusion, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicant respectfully requests that the Examiner call

the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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